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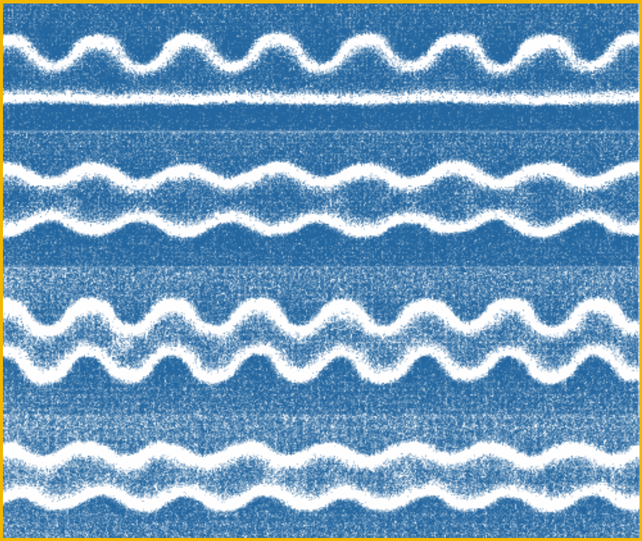

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# MATCHING PROPERTIES OF DEEP SUB-MICRON MOS TRANSISTORS

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# Contents

# Preface

This book examines the matching properties of deep sub-micron MOS transistors. Microscopic fluctuations cause stochastic parameter fluctuations that affect the accuracy of the MOSFET. For analog circuits this determines the trade-off between speed, power, accuracy and yield. Furthermore, due to the down-scaling of device dimensions, transistor mismatch has an increasing impact on digital circuits. Good insight in the magnitude of the fluctuations and their physical origins is therefore required.

This work studies the matching properties of MOSFETs at several levels of abstraction. Firstly, a simple and physics-based model is presented that accurately describes the mismatch in de drain current for the full bias range above the threshold voltage. This facilitates accurate circuit design for deep sub-micron technologies. Secondly, the most commonly used methods to extract the matching properties of a technology are bench-marked with respect to model accuracy, measurement accuracy and speed, and physical contents of the parameters. This creates insight in which method to use in which situation and in how to treat data presented in literature. As third topic the physical origins of microscopic fluctuations and how they affect MOSFET operation are investigated. This leads to a refinement of the generally applied $\sigma_{\Delta P} \propto 1/\sqrt{area}$ law in both weak and strong inversion. In addition, the analysis of simple transistor models highlights the physical mechanisms that dominate the fluctuations in the drain current and transconductance. The fourth topic considers the impact of process parameters on the matching properties. In accordance with literature, it is found that the granular structure of the poly-silicon gate material can play an important role. Furthermore, it is identified that the gate does not act as an ideal mask for the halo implantation, which worsens the matching properties of a technology. Also, scaling issues are briefly addressed. Finally, the impact of gate line-edge roughness is investigated, which is considered to be one of the roadblocks to the further down-scaling of the MOS transistor. The impact of line-edge roughness on parameter fluctuations, off-state current and yield has been modeled. The effect has also been experimentally studied by intentionally increasing the roughness and by studying transistors with sinusoidally shaped gate edges. A prediction is made about the technology node at which line-edge roughness will become an issue. Summarizing, regarding the matching properties of deep sub-micron MOS transistors, this book tries to present insight in the modeling aspects, characterization aspects, the physical origins, and technological aspects, while also extensively treating one of the main future issues. This work could therefore be useful for device physicists, characterization engineers, technology designers, circuit designers, or anybody else interested in the stochastic properties of the MOSFET.

# Acknowledgments

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The work on line-edge roughness would not have been possible without the help of Peter Leunissen. I greatly appreciate our discussions on the fundamental aspects of the topic, setting up the experiments and the time he spent on creating the required test structures.

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Jeroen Croon
November 2004

# Chapter 1

# INTRODUCTION

No two transistors are the same. When closely examined, differences can be observed at several levels, that, in one way or the other, are related to distance. For instance, when two 'identical' circuits are not fabricated in the same facility, they are produced by different people using different machines. This results in slightly nonidentical circuits and different circuit yields for the two different plants. In order to minimize differences, strategies like the 'copy EXACTLY! technology transfer method' of INTEL can be employed [1]. However, even within one production facility, differences between 'identical' circuits are observed. Different lots are not always processed using the same machines, while a machine itself shows a slight drift in time, which causes differences between wafers. On a single wafer, differences between dies are observed, which are called inter-die variations. These could for example be due to the fact that during processing the temperature is slightly different at the edge of a wafer than at its center.

The above effects are summarized in figure 1.1. The variation between circuits increases as their distance at process time increases. At the bottom of the upturned pyramid the intra-die fluctuations are present. Intra-die fluctuations are the differences between supposedly identical structures within one die. These differences can have a systematic nature when they are caused by asymmetries in layout. For instance, it was shown in [2] that the proximity of metal wiring lines can affect transistor operation. This e.g. reduces the mirror factor of a current mirror when one of the two transistors is more closely located to the metal line, which needs to be taken into account when the circuit is designed.

Besides systematic mismatch, also a stochastic component is present

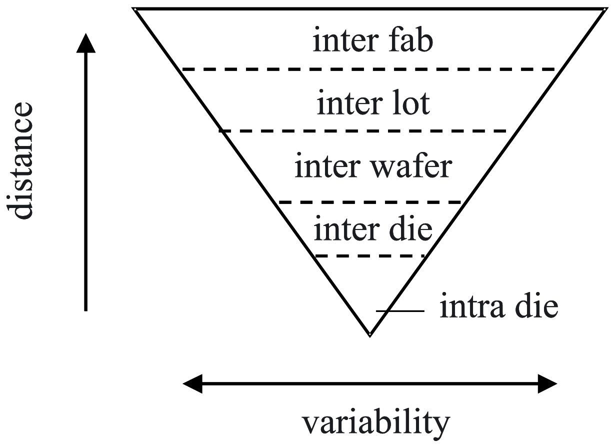

*Figure 1.1.* Variability at several levels

that is caused by the fact that at the microscopic level[1] transistors are not the same. One of the most well known examples of stochastic fluctuations in MOSFETs is the random nature of the amount of dopant atoms and their positions [3]. Stochastic fluctuations are independent of the distance between the devices under study, and by this they determine the maximal obtainable accuracy within a certain technology. In this work, we study the stochastic fluctuations of the MOSFET, which is the most important component of modern-day integrated circuits.

## 1.1 Matching analysis

The overall variability of a component is the sum of the variabilities at all levels. When studying the stochastic component, we want to filter out all other possible causes of variation. This is achieved by matching analysis, which characterizes the difference between two devices. Consider figure 1.2, which shows two types of variation: 1) Microscopic fluctuations typically have a length scale that is shorter than the device dimensions, and can be considered as spatial noise. 2) The other types of variations have length scales that are longer. Now look at the differences between the three devices that are depicted in figure 1.2. The difference between the first and third device is for the largest part due to a disturbance close to device 3, of which the impact lessens as distance increases. In other words, because the surroundings of device 1 and device 3 are nonidentical, their behavior is also nonidentical. This is often caused by

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[1] Or at the nanoscale level for modern-day devices.