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Shmuel Wimer

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*To our many Intel colleagues and friends,  
who taught us and learned from us.*





# Preface

Interconnect has become a crucial element in advanced electronic systems. State-of-the-art CMOS processes utilize 10 or more layers of metal above the active transistors, so these interconnect layers dominate processing costs. In recent years, *interconnect power* and *interconnect delay* have become major limiters for VLSI technology. Interconnect engineering—designing on-chip wires to satisfy performance requirements while meeting power, reliability, and cost specifications—is currently one of the most challenging tasks faced by product development teams. Significant difficulties arise because traditional approaches to the physical design of wires do not capture the interaction among multiple nets in complex interconnect structures.

While the downscaling of device sizes led to continuous improvement in the properties of transistors, it caused significant degradation in properties of the metal wires that are used as system interconnects. Wires have become limiters of speed, power dissipation, and reliability because of their growing resistance and capacitance in scaled fabrication processes. Interconnect issues have major implications on circuit architecture, design methodologies, and CAD tools. Timing/power/noise trade-offs have become interconnect centric, hence such trade-offs must be made during placement and routing of cells and wires.

Due to nonuniform scaling of wire thickness and wire width, net-to-net cross-capacitance between adjacent wires constitutes the largest part of total interconnect capacitance. Line-to-line cross-capacitances within the same metal layer are important determinants of speed and power so that mutual effects between parallel adjacent wires must be considered during the physical design of the circuit layout. Consequently, the spacing distance between wires on the chip has become a highly important resource, which deserves careful allocation and optimization. Since each space represents mutual interaction between two adjacent wires, simultaneous

optimization of multiple wires is called for. However, tools and methodologies for VLSI layout generation typically work net by net, handling a single wire at a time.

This book integrates our research, our industrial experience, and our teaching experience in the field. It is focused on *simultaneous optimization of multiple nets*, considering the mutual interaction between wires. New techniques for layout migration and optimization are presented, employing *multinet optimization*. The interconnect layout area in each metal layer is regarded as a common resource shared by the wires. Multinet optimization allocates this resource by applying novel algorithms based on unique properties of the optimization problems considered. The material includes optimization under discrete (gridded) design rules for advanced lithography processes. Mathematical properties and conditions for optimality of multiwire layout structures are derived, algorithmic solutions are described and analyzed, design automation flows are described, and industrial examples in advanced nanoscale technology are presented.

The book is comprised of three major parts. The first part includes background material and introduction to the field, the second part is mostly a survey of classical net-by-net optimization techniques in VLSI circuit design, and the third part covers research on multinet optimization.

In the first part of the book, evolution of the interconnect scalability problem is described in Chapter 1 from both theoretical and practical viewpoints. In Chapter 2, interconnect aspects in design methodology and CAD tools are briefly reviewed, primarily for readers who are not familiar with practical details of layout design. In Chapter 3, a tutorial of scaling theory and electrical modeling of interconnects is given.

In the second part, Chapter 4 provides a classification of optimization problems and solution techniques in interconnect layout design, emphasizing the overall differences between net-by-net approaches and multinet approaches, and stressing the advantages of the latter approach. Chapter 5 contains a concise summary of methods in net-by-net interconnect and circuit optimization, covering both classical results and recent research results, such as a new unified logical effort theory.

The third and largest part of the book consists of Chapters 6–9, covering new multinet optimization approaches. Chapter 6 is focused on a simple (but very common) layout structure called a *bundle* of wires. It is simply a set of adjacent equal-length parallel wires in a single layer. Due to its simplicity, this specific layout pattern provides good insight, analytic results, and properties that are useful for optimizing various design objectives where the optimization variables are the individual *wire widths* and the *spaces* between adjacent wires. In Chapter 7, the same optimization problems are applied to *general wire layouts* rather than bundles, where the generalized wire structure is described by a visibility graph. In Chapter 8, the simple bundle of wires is revisited, but a different kind of optimization is used, namely, *reordering of the wires* within the bundle in addition to sizing and spacing. In Chapter 9, a hierarchical solution is presented for the problem of *layout migration*. The contribution of Ron Pinter and Yuval Shaphir to this chapter is hereby gratefully acknowledged. In Chapter 10, future research and development directions in interconnect design are outlined.

For us, this book is a summary of many exciting endeavors performed over many years of work in this field. We hope it will help students, researchers, and engineers and inspire them to find creative solutions to system interconnect issues in future generations of technology.

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# Contents

<b>1</b>	<b>An Overview of the VLSI Interconnect Problem . . . . .</b>	<b>1</b>
1.1	Driving Forces: Economy and Technology . . . . .	1
1.2	Complexity and Connectivity: A System Architect's View . . . . .	2
1.3	Complexity and Connectivity: A Process Technologist's View . . . . .	4
1.4	The Interconnect Scaling Problem . . . . .	5
1.5	Implications of the Interconnect Scaling Problem . . . . .	7
1.6	The Value of Multi-net Optimization . . . . .	8
<b>2</b>	<b>Interconnect Aspects in Design Methodology and EDA Tools . . . . .</b>	<b>11</b>
2.1	Interconnect Planning . . . . .	11
2.2	Interconnect Synthesis . . . . .	13
2.3	Final Generation of Interconnect Layout . . . . .	15
2.4	Future Requirements for Interconnect Synthesis . . . . .	15
<b>3</b>	<b>Scaling Dependent Electrical Modeling of Interconnects . . . . .</b>	<b>17</b>
3.1	Technology Scaling . . . . .	17
3.1.1	Scaling of Transistors . . . . .	17
3.1.2	Scaling of Interconnects . . . . .	18
3.2	Circuit Models of Interconnect . . . . .	18
3.2.1	Ideal Interconnect . . . . .	19
3.2.2	Capacitive Interconnect . . . . .	20
3.2.3	Resistive Interconnect . . . . .	21
3.2.4	Resistive Interconnect Trees . . . . .	22
3.3	Scaling Effects on Interconnect Delay . . . . .	26
3.4	Cross-Capacitances and Their Decoupling with Miller Factor . . . . .	28
3.5	Interconnect Power . . . . .	30
3.6	Interconnect Noise (Crosstalk) . . . . .	31

<b>4</b>	<b>Frameworks for Interconnect Optimization</b> . . . . .	35
4.1	Net-by-Net Optimization . . . . .	35
4.2	Multi-net Optimizations . . . . .	38
4.2.1	Bundle of Wires . . . . .	38
4.2.2	General Wire Layouts with a Preferred Direction . . . . .	40
4.2.3	Optimization by Wire Ordering . . . . .	41
4.2.4	Interconnect Optimization in Automated Layout Migration . . . . .	41
4.2.5	Summary of Interconnect Optimization Frameworks . . . . .	41
<b>5</b>	<b>Net-by-Net Wire Optimization</b> . . . . .	43
5.1	Single-Stage Point-to-Point Wires . . . . .	43
5.1.1	Stage Delay with Capacitive Wire (Negligible Wire Resistivity) . . . . .	43
5.1.2	Stage Delay with Resistive Wire . . . . .	45
5.1.3	Repeater Insertion . . . . .	46
5.1.4	Wire Sizing (Tapering) . . . . .	47
5.2	Multistage Logic Paths . . . . .	52
5.2.1	Logical Effort Optimization . . . . .	52
5.2.2	Logic Gates as Repeaters . . . . .	54
5.2.3	Unified Logical Effort – Combined Optimization of Gates and Wires . . . . .	54
5.3	Tree-Structured Nets . . . . .	60
<b>6</b>	<b>Multi-net Sizing and Spacing of Bundle Wires</b> . . . . .	63
6.1	The Interconnect Bundle Model . . . . .	63
6.2	Power, Delay and Noise Metrics for a Bundle of Parallel Wires . . . . .	66
6.2.1	Calculating Parameters of Effective Driver and Effective Load . . . . .	66
6.2.2	The Role of Cross-Capacitance in Delay and Power Calculations for a Bundle of Parallel Wires . . . . .	68
6.2.3	Power and Delay Objectives for Optimizing a Bundle of Wires . . . . .	71
6.3	Bundle Spacing and Sizing with Continuous Design Rules . . . . .	73
6.3.1	Optimizing the Total Power of a Wire Bundle . . . . .	73
6.3.2	Optimizing the Total Sum (or Average) of Delays (Slacks) . . . . .	75
6.3.3	Minimizing Maximal Delays and Negative Slack: MinMax Problems . . . . .	78
6.3.4	Iterative Algorithm for MinMax Delay or Slack . . . . .	81

6.3.5	The Relation Between the Minimal Total Sum and MinMax Solutions . . . . .	82
6.4	Bundle Spacing and Sizing with Discrete Design Rules . . . . .	90
6.4.1	Introduction to Discrete Design Rules Problems . . . . .	91
6.4.2	Formal Definition of Discrete-Rule Bundle Problems . . . . .	92
6.4.3	Discrete Width and Space Allocation in Homogeneous Interconnect Bundle . . . . .	95
<b>7</b>	<b>Multi-net Sizing and Spacing in General Layouts</b> . . . . .	<b>107</b>
7.1	A One-Dimensional Single Objective Spacing Problem . . . . .	109
7.1.1	Problem Definition . . . . .	109
7.1.2	Necessary and Sufficient Conditions for Minimal Power . . . . .	111
7.1.3	A Graph Model for the Spacing Problem . . . . .	115
7.1.4	An Algebraic Solution for Power Minimization . . . . .	119
7.1.5	Iterative Algorithms for Power Minimization . . . . .	120
7.1.6	Maintaining Delay Constraints while Minimizing Power . . . . .	125
7.2	Optimization of the Weighted Power-Delay Objective . . . . .	129
7.2.1	Problem Definition . . . . .	129
7.2.2	Solution of the Optimal WPDS . . . . .	133
7.2.3	Practical Considerations in Power-Delay Optimization . . . . .	134
7.3	Optimizing All the Layers Together . . . . .	136
7.3.1	Timing InterDependency Between Wire Segments in a Net . . . . .	136
7.3.2	Nonoptimality of Wire-by-Wire Optimization . . . . .	137
7.3.3	All-Layers Optimization Problem Definition . . . . .	140
7.3.4	Algorithm for a Solution of the Optimal Spacing Problem . . . . .	148
7.3.5	Practical Considerations . . . . .	152
7.3.6	Layout Separation . . . . .	153
7.3.7	Examples and Experimental Results . . . . .	155
7.4	Discussion on the Optimization of General Layouts with Discrete Design Rules . . . . .	159
7.4.1	A Graph Model of Wire Width and Space . . . . .	159
7.4.2	Complexity Analysis . . . . .	163
7.4.3	Implementation and Experimental Results . . . . .	164
	Conclusion . . . . .	165
<b>8</b>	<b>Interconnect Optimization by Net Ordering</b> . . . . .	<b>167</b>
8.1	Problem Formulation . . . . .	169
8.2	The Optimality of Symmetric Hill Order . . . . .	171