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Memristor-Based Nanoelectronic Computing Circuits and Architectures

Foreword by Leon Chua

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to my wife Evelyn with love
I.V.
to my family: Stella, Marina, and Christos for their love and support
G.S.

Foreword

The memory-resistor (memristor) is a two-terminal electronic device, defined by a state-dependent Ohm's law; its resistance depends on a set of internal state-variables. The favorable circuit properties of memristors justify the recent explosive growth of related research efforts which led to several advancements in theory and potential unique applications of memristors including, among others, computing.

Currently there are only a few available book titles devoted to memristors. Vourkas and Sirakoulis in *Memristor-Based Nanoelectronic Computing Circuits and Architectures* bring together a series of memristor-related topics which are studied and presented for the first time in a single volume, i.e. device modeling, complex device interconnections, logic and memory circuits, as well as computing circuits and systems where the memristors are used either as two-state switches or as analog devices. More specifically, the book consists of eight main chapters. Chapter 1 deals with the foundations of memristor theory and the fundamental properties of memristors. Chapter 2 is devoted to modeling of voltage-controlled bipolar memristors and describes a threshold-type SPICE-compatible device model, on which the authors based the simulations and research findings shown in the rest of the book. Chapter 3 focuses on complex memristor interconnections and studies the composite emerging behavior with application in memristive multi-state switches. Chapter 4 addresses design strategies for digital logic circuits with memristors, passing from sequential stateful logic to new circuit design schemes which allow for parallel processing of the applied inputs. Chapter 5 is dedicated to crossbar-based information storage systems, studying alternative memory cells and architectural aspects which could lead to more reliable memristor memories. In the same context, Chapter 6 integrates the memristive multi-state switches of Chap. 3 with the crossbar circuit geometry in a multi-level memristor-based crossbar memory, which is then used in an early approach to memristor-based high-radix arithmetic logic units (ALU). Chapter 7 studies the emerging parallel computing capabilities of complex two-dimensional memristor networks and presents a novel methodology to efficiently map oriented graphs onto memristive networks, using

circuit models which cover a variety of connection types between graph vertices. Finally, Chapter 8 presents a circuit-level Cellular Automata (CA)-inspired methodology for computational schemes which are applied to solve several NP-hard problems of various areas of artificial intelligence (AI).

All the parts of the book are written in a simple language accessible by scientists, researchers, engineers, as well as young undergraduates. This book title is unique and timely, providing a comprehensive study which spans from memristor fundamental theory, device modeling and device interconnections, to circuit-level and system-level digital/analog applications. It includes several new results originating from the research endeavor of the authors in this very promising and highly multidisciplinary scientific field. At the moment, there is not any competitive title which deals with the range of the provided here memristor-related research in a truly compact form, which is why *Memristor-Based Nanoelectronic Computing Circuits and Architectures* can be a valuable textbook for undergraduate and postgraduate students.

Berkeley, USA Leon Chua

Preface

Motivation

Continued dimensional and functional scaling of Complementary Metal-Oxide-Semiconductor (CMOS) technology is driving information processing into a broadening spectrum of new applications. Many of these applications are enabled by performance gains and/or increased complexity realized by scaling. The performance of the components and the final application can be measured in many different ways; higher speed, higher density, lower power, more functionality, etc. Traditionally, though, dimensional scaling had been adequate to bring about these performance merits but it is no longer so. Since dimensional scaling of CMOS will eventually approach fundamental limits, several new alternative information processing devices and architectures for existing or new functions are being explored to sustain the historical integrated circuit scaling cadence and the reduction of cost/function in the next decades [1].

CMOS logic and memory together form the predominant majority of semiconductor device production. Today the semiconductor industry is facing two classes of difficult challenges related to extending integrated circuit technology to new applications and to beyond the end of CMOS dimensional scaling. One class relates to pushing CMOS beyond its ultimate density and functionality by integrating a new high-speed, highly-dense, and low-power memory technology onto the CMOS platform. The other class is to extend information processing substantially beyond that attainable by CMOS, using an innovative combination of new devices, interconnect and architectural approaches for extending CMOS and eventually inventing a new information processing platform technology. Difficult challenges gating the development of emerging research devices are therefore divided into two parts: (i) those related to memory technologies, and (ii) those related to information processing or logic devices.

The semiconductor industry is definitely in need of a new memory technology that combines the best features of current memories in a fabrication technology compatible with the CMOS process flow, scaled beyond the present limits of SRAM and Flash. This would provide a memory device fabrication technology required for both stand-alone and embedded memory applications. For DRAM, currently the main goal is to continue to scale the foot-print of the 1T-1C cell to the practical limit of $4F^2$, where F is the minimum feature size. Some issues concern vertical transistors, new dielectrics which improve the capacitance density, and keeping the leakage currents low. The requirement of low leakage currents, however, causes problems in obtaining the desired access transistor performance. A revolutionary solution of having a capacitor-less cell would be highly beneficial. Regarding nonvolatile memory (NVM), the current mainstream is Flash memory. Dense, fast, and low-power NVM is becoming highly desirable in computer architecture. However, there are serious issues with scaling of Flash memories. 2D Nand-type Flash should stay dominant for as far as it can scale because it is a well-established technology and has a very simple structure, requiring only one transistor. Ultimate density scaling may require 3-D architecture, such as vertically stackable cell arrays with acceptable yield and performance. 3-D Nand Flash is currently being developed but cost-effective implementation of this new technology, along with multi-level cell and acceptable reliability, remains a difficult challenge. Consequently, since the ultimate scaling limitation for charge-based storage devices is too few electrons, devices that provide memory states without electric charges are promising to scale further.

Moreover, as mentioned before, a major portion of semiconductor device production is devoted to CMOS digital logic, both high-performance and low-power, which is typically for mobile applications. A longer-term challenge is therefore the invention of a producible information processing technology addressing “beyond CMOS” applications. For example, emerging research devices might be used to realize special purpose processing units that could be integrated with multiple CMOS components to obtain performance advantages. These new special purpose units may provide a particular system function much more efficiently than a digital CMOS block, or they may offer a uniquely new function not available in a CMOS-based approach. A new information processing technology must also be compatible with a system architecture that can fully utilize the new device. Possibly, a non-binary data representation and/or non-Boolean logic may be required to employ a new primitive device for information processing.

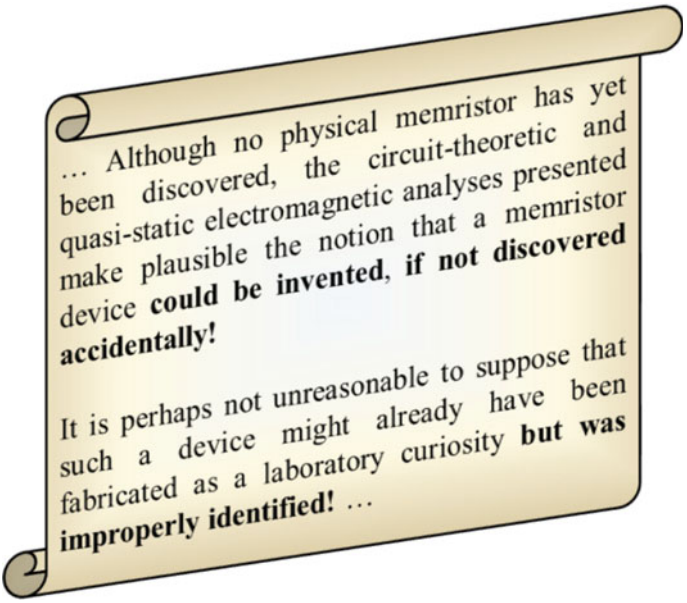
All aforementioned requirements are currently driving the industry towards a number of major technological innovations, including material and process changes, as well as totally new circuit structures. There is a growing interest in new devices for information processing and memory, new technologies and new paradigms for system architecture. Solutions to all these challenges could also lead to

new opportunities for an emerging research device technology to eventually replace CMOS as a mainstream information processing technology, provided that it possesses most of (if not all) the mentioned desirable performance merits. To this end, resistive-switching devices known as "memristors" or "memristive devices" have become the focus of many research efforts by academia and industry lately. Their advantageous performance characteristics render them a candidate technology able to bring the next technological revolution in electronics, while serving as a bridge between CMOS and the realm of nanoelectronics beyond the end of CMOS dimensional and equivalent functional scaling.

Memristor: A Promising Emerging Nanoelectronic Device

As a result of his preliminary exceptional work in nonlinear circuit theory during the 1960s, in 1971 Prof. L.O. Chua made an interesting observation that led to his discovery of the memristor as a mathematical entity [2]. For completely linear circuits there are only three independent two-terminal passive circuit elements: the resistor R, the capacitor C, and the inductor L, which are defined axiomatically via a constitutive relation between a pair of variables chosen from {v (voltage), i (current), q (charge), φ (flux linkage)}. There are six different pairs than can be formed from these four variables, namely {(v, φ), (i, q), (v, i), (v, q), (i, φ), (φ, q)}, and five of them were already related mathematically. However, when Chua generalized the mathematical equations to be nonlinear, there was another independent differential relationship that in principle coupled the charge q that flowed through the circuit and the *flux linkage* (time-integral of the applied voltage) φ as in $d\varphi = Mdq$, different from the resistance which coupled the voltage v to the current i, $dv = Rdi$.

He mathematically explored the properties of this new nonlinear circuit element and found that it was essentially a "resistor with memory", so he called it a memristor M; it was a two-terminal device that changed its resistance according to the amount of change that flowed through it. This prediction of the properties of a new "missing" (by that time) circuit element from symmetry principles was absolutely revolutionary; more importantly, it did not depend on any experimental observation but it was rather a result of curiosity. As Chua himself declared in his 1971 paper, it was not obvious at that time that a physical analog of such circuit element existed; the attached text below is a summary of what is stressed in the original paper (last paragraph on page 519 of [2]).



The reason why memristors are substantially different from the other fundamental circuit elements is that, when you turn off the voltage to the circuit they still remember how much voltage was applied before and for how long, thus presenting a memory of their past. That's an effect that can't be duplicated by any circuit combination of resistors, capacitors, and inductors, which qualifies the memristor as a fundamental circuit element.

Today we know that memristors are ubiquitous and many devices, including the "electric arc" which dates back to 1801, have been identified as memristors. Indeed, there had been experimental clues to the memristor's existence all along the last two centuries. Scientists have been publishing in the literature experimental results with "strange" voltage characteristics, where one sees clearly memristance, though such a material property had always been shadowed by other effects that were of primary interest [3]. In the absence of an application, there was no particular need to seek memristive behavior anyway. After the publication of Chua's seminal paper, the connection between many strangely behaving components and his original theoretical definition was not made at least for three decades by then. The memristor had been relegated as an abstract device with no practical significance until 2008 when Chua's theory of memristor was successfully linked to its first "modern" practical nanoscale implementation by a group at Hewlett Packard (HP) Laboratories [4]. Their seminal Nature paper originated intense research activity in this novel scientific field and generated unprecedented worldwide interest for the potential applications, with publications increasing at an exponential rate ever since.

Memristor exhibits its unique properties primarily at the nanoscale. Therefore, much of the recent research work has focused on the technological side concerning

the physical realization of such devices for a better understanding of the physical principles and their tuning. Currently, there is a growing variety of systems that exhibit memristive behavior, as academia and industry keep on with their research and prototyping [5, 6]. Among them, molecular and ionic thin film memristive systems primarily rely on different material properties of thin film atomic lattices that exhibit hysteresis under the application of charge. In experimentally realizable systems, memristive devices with threshold voltages seem to be the norm rather than the exception, and electronic conduction is in most cases dominated by an effective tunneling barrier—width that varies with the applied voltage.

The memristor creates a new opportunity for realization of innovative circuits that in some cases are not possible or have inefficient realization in the present and established design domain. It provides many advantages such as scalability down to sub-10 nm, nonvolatility, fast switching speed, energy efficiency, and CMOS compatibility, just to name a few; thus it is believed to bring a new wave of innovation in electronics, supplanting or supplementing transistors in several applications, while it might bring analog information processing back into the world of computing. Memristor-based circuits open new pathways for the exploration of advanced computing architectures as promising alternatives to conventional integrated circuit technologies, which are facing serious challenges related to continuous scaling [1]. Most importantly, memristors provide an unconventional computation framework, different from familiar paradigms, which combines information processing and storage in the memory itself; i.e. the major distinction from the present day's computing technology [7]. Such framework is determined more by the device properties than any previously conceived logic paradigm.

Amongst several emergent applications of the memristance switching phenomenon, implementation of logic circuits is gaining considerable attention. In binary digital circuits, memristors would operate as two-state switches, toggling between max and min resistance. Using memristors for digital processing has the advantage of combining storage and logic functionality with the same technology in one single device. However, the widest field of proposals on how to use memristors for processing concerns analog computing. If several intermediate resistive states could be distinguished reliably, then the information density could be raised to more than one bit per device, but the end point of this evolution is to be able to fully exploit the analog nature of memristors. For example, using the possibility to store a ternary value in one physical storage cell allows building up a better arithmetic unit as is fundamentally possible and actually done with conventional binary logic. Anyway, active components such as transistors would still be needed even if most information processing were done by memristors. One reason is that signals are reduced in amplitude by every passive circuit element and, at some point, they must be restored. Another reason might concern accessing memristors for reading/programming their state. Hybrid circuits that combine memristors and active elements are a lively area of investigation, whereas the distinct properties of memristive devices might even lead to *neuromorphic* computer systems in the future [8].

Up to now, the fabrication of digital memories is the driving force of memristor technology, since very dense memory architectures can potentially be manufactured. Rapid progress in the advancements of memristive technology is reflected in the early commercialization of memristive memory (resistive RAM—ReRAM) products [9]. Such activity together with the groundbreaking announcement of "the Machine" by HP on June 2014 [10], prove the ever-increasing interest and active involvement of industry leading companies in the future production of memristor-related products and pioneering memristive computing architectures. The continuous improvement of the memristance switching behavior, thanks to the incessant accumulation of knowledge on resistive switching materials and the underlying phenomena, is encouraging for the future implementation and establishment of unconventional computing paradigms and sophisticated memristive circuits and systems. But whether the memristor will finally fulfill all these hopes remains to be seen; in order to evaluate long-term prospects of such technologies one would have to go beyond the basic principles and to questions of reliability, variability, manufacturing cost, etc.

The content of this book spans from fundamental device modeling to emerging storage system architectures and novel circuit design methodologies, targeting advanced non-conventional analog/digital massively parallel computational structures. Effective modeling is the first step towards a deeper understanding of the memristive dynamics and the better exploitation of their unique properties for potential utilization in a variety of emerging applications. Well defined and effective SPICE-compatible memristor models, as those presented in Chap. 2, would certainly accelerate research in memristive circuits and systems. Also, while most of the research has so far focused on the properties of single memristors, very little is known about their response when they are organized into networks. Composite memristive systems built out of networks of individual memristors, demonstrate different electrical characteristics from their structural elements due to their threshold-dependent nonlinear resistance switching behavior. Therefore, their rich and dynamic overall behavior could be exploited for the creation of novel sophisticated memristive circuits and systems with multi-bit storage per device capabilities. Collective memristive dynamics is the focus of Chaps. 3, 7, and 8, whereas the same property is the basis for the design of memristor-based logic circuits in Chap. 4. Furthermore, nonvolatile resistive RAM (ReRAM) is nowadays considered as one of the promising alternatives to current baseline memory technologies. At the architectural level, crossbar memory cell array structure offers several benefits and is considered one of the best ways to implement ReRAM of highest possible device density. However, a typical passive crossbar memory suffers from the existence of parasitic conducting (current sneak paths) reducing both the size and the reliability of the memory. Innovative approaches to memory cell structure and memory architecture, which will efficiently address the current sneak-path problem, constitute nowadays a key factor towards the practical realization of passive crossbar-based ReRAM and reflect the content of Chap. 5.

Moreover, a great effort was placed towards the creation of relevant design automation/simulation tools and proper methodologies which address important current technological drawbacks and thus enable/facilitate the development of efficient design flows for reliable circuits and architectures comprising memristors. Such tools are presented in Chaps. 4 and 5. Furthermore, it has been well-known for a long time that faster arithmetic operations could be achieved via high-radix numeric systems [11]. However, in the absence of appropriate storage devices, such practice was not given much attention because it would require doubling the memory capacity to represent high-radix numbers in binary mode. In Chap. 6 we present a novel method for implementing crossbar-based multi-level memories, where each cross-point cell stores multiple bits. Furthermore, we propose a conceptual solution for novel CMOS-compatible, memristive, high-radix arithmetic logic units (ALUs) for future computing systems.

The extensive study of memristive nanoelectronic circuits and architectures presented within this book is indicative of the fast pace of this novel and intriguing field. High-density memristive data storage combined with memristive circuit-design paradigms and computational tools applied to solve NP-hard artificial intelligence (AI) problems, as well as memristive arithmetic-logic units, certainly pave the way for a much promising memristive era in electronic computing systems. The graph-based NP-hard problems are depicted to memristive networks and coupled with Cellular Automata (CA)-inspired computational schemes that enable computation within memory. The following chapters may constitute an informative cornerstone for researchers and scientists, as well as a comprehensive reference to the more experienced readers, hoping to stimulate further research on memristive devices, circuits, and systems.

Book Outline

Below there is a short summary of the following chapters which highlights the original contributions of this book to the *state-of-the-art*.

Basic theoretical definitions and general properties of memristors and memristive systems are shortly presented in Chap. 1. All necessary information for the purposes and the complete comprehension of the content of this book is provided.

In Chap. 2, the device characteristics of thin-film memristors are considered and a novel, SPICE-compatible, generic, threshold-type switching model of a two-terminal voltage-controlled bipolar memristor is presented, explaining the memristive behavior of the device by investigating the occurrence of quantum tunneling.

A rigorous study of the switching response of composite memristive systems, consisting of multiple memristors connected in complex circuit configurations, is presented in Chap. 3. A methodology for the construction of composite memristive devices, which comply with certain design specifications and facilitate the design of nanoelectronic circuits with multi-state switches, is presented. Particular application