

Studies in Systems, Decision and Control 37

Saleem Mohammed Ridha Taha

# Reversible Logic Synthesis Methodologies with Application to Quantum Computing

 Springer

# **Studies in Systems, Decision and Control**

Volume 37

## **Series editor**

Janusz Kacprzyk, Polish Academy of Sciences, Warsaw, Poland  
e-mail: [kacprzyk@ibspan.waw.pl](mailto:kacprzyk@ibspan.waw.pl)

### *About this Series*

The series “Studies in Systems, Decision and Control” (SSDC) covers both new developments and advances, as well as the state of the art, in the various areas of broadly perceived systems, decision making and control—quickly, up to date and with a high quality. The intent is to cover the theory, applications, and perspectives on the state of the art and future developments relevant to systems, decision making, control, complex processes and related areas, as embedded in the fields of engineering, computer science, physics, economics, social and life sciences, as well as the paradigms and methodologies behind them. The series contains monographs, textbooks, lecture notes and edited volumes in systems, decision making and control spanning the areas of Cyber-Physical Systems, Autonomous Systems, Sensor Networks, Control Systems, Energy Systems, Automotive Systems, Biological Systems, Vehicular Networking and Connected Vehicles, Aerospace Systems, Automation, Manufacturing, Smart Grids, Nonlinear Systems, Power Systems, Robotics, Social Systems, Economic Systems and other. Of particular value to both the contributors and the readership are the short publication timeframe and the world-wide distribution and exposure which enable both a wide and rapid dissemination of research output.

More information about this series at <http://www.springer.com/series/13304>

Saleem Mohammed Ridha Taha

# Reversible Logic Synthesis Methodologies with Application to Quantum Computing

 Springer

Saleem Mohammed Ridha Taha  
Electrical Engineering Department, College  
of Engineering  
University of Baghdad  
Baghdad  
Iraq

ISSN 2198-4182                      ISSN 2198-4190 (electronic)  
Studies in Systems, Decision and Control  
ISBN 978-3-319-23478-6              ISBN 978-3-319-23479-3 (eBook)  
DOI 10.1007/978-3-319-23479-3

Library of Congress Control Number: 2015949475

Springer Cham Heidelberg New York Dordrecht London  
© Springer International Publishing Switzerland 2016

This work is subject to copyright. All rights are reserved by the Publisher, whether the whole or part of the material is concerned, specifically the rights of translation, reprinting, reuse of illustrations, recitation, broadcasting, reproduction on microfilms or in any other physical way, and transmission or information storage and retrieval, electronic adaptation, computer software, or by similar or dissimilar methodology now known or hereafter developed.

The use of general descriptive names, registered names, trademarks, service marks, etc. in this publication does not imply, even in the absence of a specific statement, that such names are exempt from the relevant protective laws and regulations and therefore free for general use.

The publisher, the authors and the editors are safe to assume that the advice and information in this book are believed to be true and accurate at the date of publication. Neither the publisher nor the authors or the editors give a warranty, express or implied, with respect to the material contained herein or for any errors or omissions that may have been made.

Printed on acid-free paper

Springer International Publishing AG Switzerland is part of Springer Science+Business Media  
([www.springer.com](http://www.springer.com))

# Preface

Traditional technologies are increasingly beginning to suffer from the increasing miniaturization and the exponential growth of the number of transistors in integrated circuits. The high rate of power consumption and the emergence of quantum effects for highly dense integrated circuits are the biggest problems in system design today and will be in the future. Reversible logic provides an alternative to face the upcoming challenges. One of the main benefits that reversible logic brings about is theoretically zero power dissipation. In order to reduce power consumption, physical processes have to be logically reversible. Every future technology will have to use reversible logic circuits in order to reduce power consumption. In the area of quantum computation and low-power design, very promising results have already been obtained today. Nevertheless, research on reversible logic is still at the beginning stage.

This book provides several novel contributions to reversible logic synthesis. Twelve reversible logic synthesis methodologies are presented for the first time in a single literature. Evaluations for the comparative advantages and disadvantages of these methodologies are also provided. Reversible sequential logic circuits are discussed, with new designs of reversible sequential elements.

The tendency of current technologies is towards the nanoscale. Therefore, there is a need to incorporate the physical quantum mechanical effects that are unavoidable in the nanoscales. Representations and operations in quantum computing that use theorems of reversible computing and reversible structures to compute functionalities using quantum logic are introduced. Applications of wavelet and multiwavelet transformations to quantum computing structures are discussed. New techniques to implement the Daubechies wavelets and multiwavelets using quantum circuits are proposed.

Finally, highlights of novel contributions that are presented in this book and the future directions of research are provided.

In this context, the contributions to this book provide a good starting point. It is hoped that this book will help to spur further research in the field of reversible and quantum computations. In fact researchers in academia or industry and graduate

students, who work in this field, will be interested in this book. Books that are concerned with reversible synthesis of logic functions are rare. Therefore, there is a need to publish books in this field. The first book [1] presented for the first time comprehensive and systematic methods of reversible logic synthesis. It is hoped that this book will be more valuable, because 12 methods of reversible logic synthesis are introduced here, while only five are in Ref. [1]. Also, for the first time the sequential reversible logic circuitries are discussed in a book.

This book opens the door to a new interesting and ambitious world of reversible and quantum computing research. It presents the state of the art, with some new proposals.

Baghdad  
January 2015

Saleem Mohammed Ridha Taha

## Reference

1. A.N. Al-Rabadi, *Reversible Logic Synthesis: From Fundamentals to Quantum Computing* (Springer-Verlag, 2004)

# Contents

<b>1</b>	<b>Introduction</b> . . . . .	1
1.1	Background . . . . .	1
1.2	What This Book Is About . . . . .	2
1.3	Motivation . . . . .	2
1.4	Major Contributions of This Book . . . . .	3
1.5	Overview of the Book Chapters . . . . .	3
1.6	Overall Message of the Book . . . . .	4
	References. . . . .	4
<b>2</b>	<b>Fundamentals of Reversible Logic</b> . . . . .	7
2.1	Preliminaries . . . . .	7
2.2	Basic Definitions . . . . .	8
2.3	Reversible Logic Gates . . . . .	9
2.3.1	Feynman Gate . . . . .	9
2.3.2	Toffoli Gate . . . . .	11
2.3.3	Fredkin Gate . . . . .	11
2.4	Reversible Logic Synthesis . . . . .	12
2.5	Overview of Reversible Logic Synthesis Methods. . . . .	12
2.6	The Elimination of Garbage in Binary Reversible Circuits . . . . .	14
	References. . . . .	15
<b>3</b>	<b>Methods of Reversible Logic Synthesis.</b> . . . . .	17
3.1	Reversible Expansions and Reversible Spectral Transforms . . . . .	17
3.1.1	Reversible Ternary Shannon and Davio Expansions. . . . .	19
3.1.2	Reversible Shannon Spectral Transforms . . . . .	21
3.1.3	Reversible Davio Spectral Transforms . . . . .	23



3.2	The Elimination of Garbage in Ternary Reversible Circuits . . . . .	26
3.3	Reversible Decision Trees (RDTs) . . . . .	29
3.4	Reversible Decision Diagrams (RDDs) . . . . .	31
3.5	Reversible Lattice Circuits . . . . .	32
3.5.1	Symmetric and Non-symmetric Functions . . . . .	34
3.5.2	Two-Dimensional Lattice Circuits . . . . .	35
3.5.3	Three-Dimensional Lattice Circuits . . . . .	37
3.5.4	Algorithms for Realizing the Shannon/Davio Expansions of Ternary Functions into 3D Lattice Circuits . . . . .	43
3.5.5	Complete Example for the Implementation of Ternary Functions Using 3D Lattice Circuits . . . . .	48
3.5.6	New Minimal Realization Method for 3D Lattice Circuits. . . . .	55
3.5.7	Lattice Circuit Synthesis Using ISID. . . . .	60
3.5.8	The Creation of Reversible Lattice Structures. . . . .	60
3.5.9	3D Ternary Davio Reversible Lattice Structures . . . . .	64
3.6	Reversible Fast Transform Circuits . . . . .	69
3.7	Group-Theoretic Representations. . . . .	78
3.8	Reversible Reconstructability Analysis Circuits. . . . .	81
3.8.1	Ternary MRA. . . . .	83
3.8.2	Reversible MRA (RMRA). . . . .	86
3.9	Reversible Programmable Gate Array (RPGA) . . . . .	87
3.9.1	Definitions . . . . .	87
3.9.2	(2 * 2) Net Structures and RPGAs . . . . .	88
3.9.3	The New Reversible Gate (SALEEM). . . . .	89
3.9.4	Novel Design of RPGA Based on the SALEEM Reversible Gate . . . . .	89
3.10	Reversible Cascade Circuits . . . . .	94
3.11	Spectral-Based Synthesis Method . . . . .	95
3.12	Transformation-Based Network Synthesis of Fredkin-Toffoli Cascade Gates . . . . .	99
3.13	Heuristic Algorithm for Reversible Logic Synthesis. . . . .	102
3.14	Constructive Synthesis of Reversible Circuits by NOT and (n - 1)-CNOT Gates . . . . .	104
3.15	Summary . . . . .	109
	References. . . . .	109
<b>4</b>	<b>Evaluation of the Reversible Logic Synthesis Methodologies . . . . .</b>	<b>111</b>
4.1	NPN-Classification of Logic Functions . . . . .	111
4.2	New Evaluation Procedure of Reversible Synthesis Methods . . . . .	112

4.3	Comparison Between the Various Reversible Synthesis Methodologies . . . . .	116
4.4	Summary . . . . .	116
	References. . . . .	117
<b>5</b>	<b>Reversible Sequential Logic Circuits . . . . .</b>	<b>119</b>
5.1	Reversible Flip Flops . . . . .	119
5.1.1	Reversible RS Flip Flop . . . . .	120
5.1.2	Reversible Clocked RS Flip Flop . . . . .	121
5.1.3	Reversible D Flip Flop . . . . .	122
5.1.4	Reversible JK Flip Flop. . . . .	123
5.1.5	Reversible T Flip Flop . . . . .	124
5.1.6	Reversible Master-Slave Flip Flop. . . . .	125
5.1.7	The Superiority of Using the SALEEM Gate in Reversible Flip Flops Design . . . . .	126
5.2	Complex Reversible Sequential Circuits. . . . .	126
5.3	Novel Reversible Sequential Elements. . . . .	129
5.3.1	New Design of Reversible T Flip Flop . . . . .	129
5.3.2	New Design of Reversible D Flip Flop . . . . .	130
5.3.3	New Design of Reversible JK Flip Flop . . . . .	130
5.3.4	New Design of Reversible Master-Slave Flip Flops . . . . .	131
5.3.5	Evaluation of the New Reversible Flip Flops . . . . .	132
5.4	Multiple-Valued Reversible Sequential Circuits. . . . .	133
5.5	Summary . . . . .	133
	References. . . . .	134
<b>6</b>	<b>Quantum Logic Circuits and Quantum Computing . . . . .</b>	<b>135</b>
6.1	Background . . . . .	135
6.2	Quantum Bits and Superposition. . . . .	137
6.3	Qubit Registers. . . . .	138
6.4	Quantum Logic Gates . . . . .	139
6.5	Quantum Logic Circuits. . . . .	141
6.6	Synthesis of Quantum Logic Circuits . . . . .	144
6.7	Binary Quantum Decision Trees and Diagrams. . . . .	145
6.8	Fundamentals of Ternary Quantum Computing. . . . .	146
6.9	Quantum Computing for the Reversible Structures . . . . .	148
	References. . . . .	149
<b>7</b>	<b>Wavelets and Multiwavelets Implementation Using Quantum Computing . . . . .</b>	<b>153</b>
7.1	Introduction . . . . .	153
7.2	Quantum Circuits for Perfect Shuffle Permutation Matrices. . . . .	154

7.3	Quantum Wavelet Algorithms. . . . .	156
7.3.1	Wavelet Pyramidal and Packet Algorithms. . . . .	157
7.3.2	Daubechies $D^{(4)}$ Wavelet Factorization . . . . .	158
7.4	Quantum Implementation of Daubechies $D^{(4)}$ Wavelet . . . . .	160
7.5	Quantum Implementation of Daubechies $D^{(4)}$ Multiwavelet . . . . .	161
7.5.1	Computation of Discrete Multiwavelet Transform . . . . .	162
7.5.2	Computation of Inverse Discrete Multiwavelet Transform. . . . .	163
7.5.3	A New Quantum Implementation of Daubechies $D^{(4)}$ Multiwavelet Transform . . . . .	163
7.5.4	A New Quantum Implementation of Inverse Daubechies $D^{(4)}$ Multiwavelet Transform. . . . .	167
	References. . . . .	170
<b>8</b>	<b>Conclusions and Future Researches. . . . .</b>	<b>171</b>
8.1	Conclusions . . . . .	171
8.2	Promising Areas of Further Researches . . . . .	173
	References. . . . .	174

# Abbreviations

1-RPL	1-Reduced Post Literal
3D	Three-Dimensional
3DTDRL	Three-Dimensional Ternary Davio Reversible Lattice
BDD	Binary Decision Diagram
CCW	Counter Clock Wise
CIN	Common Indices Nodes
CNOT	Controlled NOT
CRA	Conventional Reconstructability Analysis
D	Davio expansion
DD	Decision Diagram
DMWT	Discrete Multiwavelet Transform
DT	Decision Tree
ESOP	EXOR Sum-Of-Product
EXOR	Exclusive-OR
GBFM	Generalized Basis Functions Matrix
GF	Galois Field
GGs	Gate–Garbage–Sum
IDMWT	Inverse DMWT
K-map	Karnough map
MRA	Modified Reconstructability Analysis
NCTSF	NOT, CNOT, Toffoli, Swap, Fredkin reversible gates
nD	Negative Davio
pD	Positive Davio
PUS	Positive Unate Symmetric
Qubit	Quantum bit
RDD	Reversible Decision Diagram
RDDT	Reversible Davio Decision Tree
RDT	Reversible Decision Tree
RGBFM	Reversible GBFM
RMRA	Reversible MRA
RPGA	Reversible Programmable Gate Array

RSGBFM	Reversible Shannon GBFM
RSPP	Rational SPP
S	Shannon expansion
S/D	Shannon/Davio
SBDD	Shared BDD
SPP	Size Power-consumption Product
T.M.	Transform Matrix
ULM	Universal Logic Modules

# Symbols

$D_{2^n}^{(4)}$	Daubechies fourth-order wavelet kernel of dimension $2^n$
$Q_{2^n}$	Downshift Permutation matrix
$\Pi_4$	Qubit Swap gate
$\Pi_{2^n}$	Perfect Shuffle Permutation matrices
$ \cdot\rangle$	Vector representing a quantum state
$\otimes$	Tensor product
$\oplus$	Modulo 2 addition
$\dagger$	Adjoint
$\equiv$	Equivalence
$\wedge$	Logical AND operator
$\vee$	Logical OR operator
$\cap$	Intersection operation

# Chapter 1

## Introduction

In this chapter, some of the background of the body of research upon which this book builds is outlined (Sect. 1.1), description (Sect. 1.2) and motivation (Sect. 1.3) of the topic of this book are explained, the major contributions of this book are summarized (Sect. 1.4), a brief overview of the contents of the later chapters is given (Sect. 1.5), and the overall message of the book is highlighted (Sect. 1.6).

### 1.1 Background

Interest in reversible logic started when Landauer in 1961 [1] proved that traditional binary irreversible gates lead to power dissipation in a circuit regardless of implementation. Each bit of information that is lost, generates  $KT \ln(2)$  Joules of heat energy, where  $K$  is Boltzmann's constant ( $\approx 1.380658 \times 10^{-23}$  J/K) and  $T$  the absolute temperature (Kelvins) at which computation is performed. For room temperature  $T$  the amount of dissipating heat is small (i.e.  $2.9 \times 10^{-21}$  J), but not negligible [2–4]. Bennett in 1973 showed that for power not to be dissipated in an arbitrary circuit, it is necessary that this circuit be built from reversible gates. The importance of Bennett's theorem lies in the technological necessity that every future technology will have to use reversible gates in order to reduce power loss [5, 6].

Reversible circuits are those circuits that do not lose information and reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping (a permutation) between input and output vectors [7, 8].

Hardware development truly took off in 1948, when the transistor was developed. Computer hardware has grown in power at an amazing pace ever since, so much so that the growth was codified by Gordon Moore in 1965 in what has come to be known as Moore's law. This law states that since the invention of the transistor the number of transistors per chip roughly doubled every 18–24 months, which means an increase in the computing power of computers [9]. This increase in computing power is due primarily to the continuing miniaturization of the elements of which computers are made, resulting in more and more elementary gates per unit