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Preface

Voltage-controlled oscillators (VCOs) and frequency dividers are two of the key building blocks in phase-locked loops (PLLs) and frequency synthesizers, not only to generate clean LO signals for frequency conversion in wireless transceivers but also to generate accurate high-frequency clock signals for wireline systems. As the system applications continue to demand higher and higher performance in terms of higher frequency, wider bandwidth, lower phase noise, and lower power consumption, the design of these building blocks becomes more and more challenging, in particular in aggressively scaled low-voltage CMOS processes for low cost and high system-on-chip integration.

Many years ago, we published a book entitled "Low-Voltage CMOS RF Frequency Synthesizers" to discuss and summarize various inductor-based design techniques for low-voltage high-performance frequency synthesizers. The main focus was on low-voltage and low-power designs for narrow-band applications, in which integrated inductors play a critical role. However, due to their high-Q and narrow-band characteristics, these design techniques have limited applications in recently emerging multi-band multi-mode and software-defined radios. Fortunately, transformer-based design techniques have recently been developed and emerged as potential replacement of integrated inductors for more features and even better performance. However, to the best of our knowledge, there has still been no book aiming to introduce transformer-based low-voltage and wideband CMOS VCOs and frequency dividers.

As continuation and complementary to our previous book and intended for engineers, mangers, researchers, and students who are working on or interested in CMOS radio frequency or mm-Wave integrated circuits and systems, this book presents in-depth description and discussion of transformer-based design techniques that enable CMOS oscillators and frequency dividers to achieve ultra-wide frequency tuning range and ultra-wide frequency locking range while maintaining state-of-the-art performance in terms of high operation frequency, low supply voltage, good phase noise, and low power consumption. In addition to the design, simulation, and characterization of integrated transformers for different

applications, this book will also discuss their unique characteristics and features that enable performance improvement, such as passive coupling or multiple impedance peaks, which have not been covered in any of the existing books. Finally, to illustrate the usefulness of these transformer-based design techniques, design consideration and optimization of various CMOS oscillators and frequency dividers for different applications together with their measured performance are elaborated, focusing on not only ultra-low supply voltage but also ultra-wide frequency tuning range and locking range at very high frequencies.

More specifically, detailed description and discussion of the following selected designs will be included in the book.

1. A transformer-feedback VCO (TF-VCO) features high swing and low phase noise even at a supply voltage below the device threshold voltage. Fabricated in a 0.18-μm CMOS process, a 1.4-GHz PMOS TF-VCO achieves an FoM of 190 at 0.35-V supply voltage, and a 3.8-GHz NMOS TF-VCO achieves an FoM of 193 at 0.5-V supply voltage.
2. A quadrature VCO using transformer coupling (TC-QVCO) eliminates both noise and power consumption by active coupling devices in existing QVCOs while exhibiting all advantages in the TF-VCO. Fabricated in a 0.18-μm CMOS process, a 17-GHz TC-QVCO achieves an FoM of 187.6 and a phase error of 1.4° at 1-V supply voltage.
3. A transformer-based dual-mode VCO achieves a wide frequency tuning range exploiting the two impedance peaks of a transformer tank. Fabricated in a 0.13-μm CMOS process, the 2.7-to-4.3 GHz and 8.4-to-12.4 GHz dual-mode QVCO achieves average FoM_T of 195 and 203 in the two bands, respectively.
4. A magnetically tuned multi-mode VCO (MT-VCO) measures ultra-wide frequency tuning range around 70 GHz by changing the coupling coefficient of the transformer. Fabricated in a 65-nm CMOS process, the 57.1-to-90.1 GHz MT-VCO achieves an average FoM_T of 188.2 at 1-V supply.
5. Transformer-feedback injection-locked frequency dividers (TF-ILFDs) feature quadrature outputs with enhanced output swing even with low supply and low power. Fabricated in a 0.18-μm CMOS process, a 18.1-GHz TF-ILFD with differential outputs achieves 21.6 % locking range when consumes 2.75–4.35 mW at 0.5-V supply, and a 17.5-GHz TF-ILFD with quadrature outputs achieves 27.8 % locking range when consuming 11.4–13.6 mW at a 0.6-V supply.
6. A self-frequency-tracking injection-locked frequency divider (SFT-ILFD) utilizing transformer to generate the injection current with frequency-dependent phase shift to extend the locking range. Fabricated in a 65-nm CMOS process, a 62.9-GHz SFT-ILFD achieves 29 % locking range while consuming 1.9 mW at a 0.8-V supply voltage.

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Chapter 1
Introduction

1.1 Motivation

Wireless and wireline transceiver systems have greatly been benefited from the aggressive scaling down of CMOS technology to improve their performance in terms of speed, power, and form factor. On the other hand, the CMOS technology scaling down also imposes great challenges to designs of radio frequency (RF) and analog circuits mainly because the supply voltage (V_{DD}) scales much faster than the threshold voltage (V_{th}) of CMOS transistors. From Fig. 1.1, the available overdrive voltage ($V_{DD}-V_{th}$) in 65-nm CMOS technology is reduced to around 0.5 V, which limits the voltage headroom and significantly degrades the performance of RF and analog circuits.

For emerging applications powered by various energy-harvesting methods, the generated supply voltage V_{DD} may be as low as or even lower than the device threshold voltage V_{th}, which limits practical use of many conventional RF and analog integrated circuits design techniques. Although on-chip boost converters can be employed to increase the supply voltage, for applications with such low input voltages and large voltage conversion ratios, their limited efficiency of around 40–75 % would cause significant power penalty [2]. Instead, exploiting RF and analog circuit techniques that can work under supply voltage close to V_{th} has been proven to be a promising solution to greatly reduce the power consumption [3].

On the other hand, emerging wireless applications utilizing much high carrier frequencies can take advantages of the large bandwidth available to provide services with data rate of multi-gigabit per second. For example, the IEEE 802.11ad (WiGig) standard [4] and IEEE 802.15.3c standard [5] located at 60 GHz provide available bandwidth of 9 GHz. However, design of wideband transceivers to cover such a large bandwidth at such a high frequency becomes quite challenging.

RF frequency synthesizers based on phase-locked loops (PLLs) to provide the local oscillation (LO) signals for frequency conversion is one of the key building

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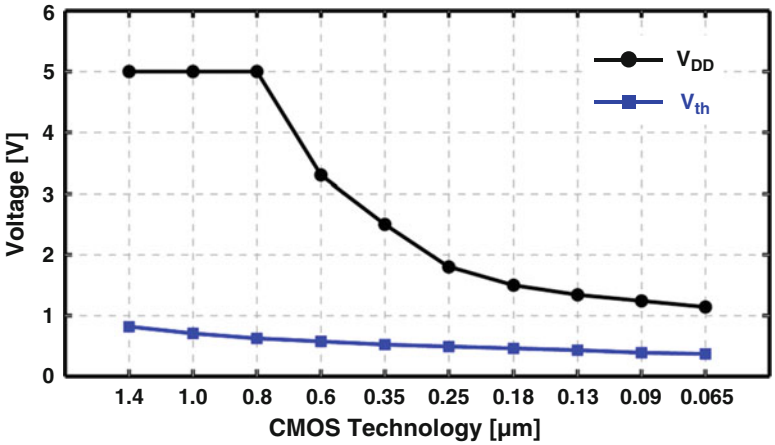

Fig. 1.1 Scaling down of supply voltage (V_{DD}) and threshold voltage (V_{th}) with the CMOS technologies [1]

blocks in wireless transceivers. The quality of the LO signals in terms of phase noise and spur would significantly affect the performance of the whole transceivers, such as the receiver sensitivity and the transmitter spurious emission. For PLLs, researches have recently focused more and more on the digital-intensive designs to make use of aggressive scaling down in CMOS technologies [6]. In digital PLLs (DPLLs), although there are digital substitutes for the phase-frequency detector (PFD), loop filter, and even frequency dividers operating at several GHz, the voltage-controlled oscillator (VCO) or the digitally controlled oscillator (DCO) still needs to be designed in the analog domain due to its high operating frequency and stringent noise performance requirement. Similarly, at millimeter-wave (mm-Wave) frequencies, the frequency dividers serving as prescalers also need to be carefully designed in the analog domain for high performance in terms of frequency, locking range, and power consumption [7].

VCOs and frequency dividers, as the two critical building blocks operating at the highest frequencies, directly affect the output frequency range and the out-of-band phase noise of the whole PLLs. LC-VCOs as shown in Fig. 1.2a are usually employed in the frequency synthesizers for wireless applications since LO signals with low out-band phase noise are required to meet the stringent blocker or spurious emission requirement for the receiver or transmitter, respectively. For the design of frequency divider, although current-mode logic (CML) dividers are fast enough for applications at giga-Hz frequency range in submicron CMOS process, injection-locked frequency dividers (ILFDs) [8, 9] with inductive tank as shown in Fig. 1.2b and c are still a necessity at mm-Wave frequencies since they feature higher operation frequencies with lower power consumption compared with CML dividers [10, 11]. For LC-VCOs and LC-ILFDs based on conventional LC tanks, their performance such as noise, operating frequency range, and driving capabilities would degrade rapidly with the scaling down of supply voltage, which limits their

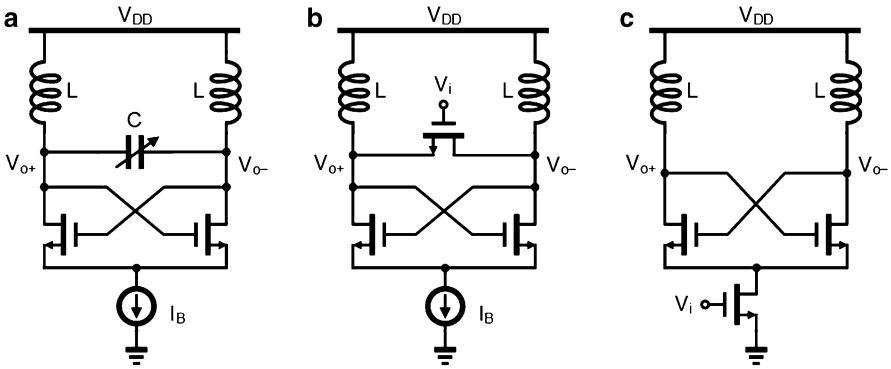

Fig. 1.2 Schematic of conventional (**a**) LC-VCO, (**b**) LC-ILFD with direct injection, and (**c**) LC-ILFD with indirection injection from current bias

usage as the CMOS technology is further scaled down. Even worse, for the applications requires a supply voltage lower than the device threshold voltage V_{th}, the conventional LC-VCOs and LC-ILFDs may fail to work properly since the cross-coupled transistors cannot provide large enough negative transconductance to compensate the loss from the LC tank.

For the design of LC tanks in conventional LC-VCOs and LC-ILFDs, high tank quality factor (Q) is preferred to suppress the noise while still maintaining low power consumption. On the other hand, the narrowband frequency response characteristics of a high-Q tank would in turn limit the operating frequency range of LC-VCOs and the locking range of LC-ILFDs. In particular, it would impose a critical challenge in modern RF transceivers that can support multi-standard and multiband applications or even the software-defined radio (SDR) and cognitive radio applications, in which ultra-wideband LOs are required. The most straightforward way to cover a wide frequency range is to duplicate multiple narrowband LC VCOs and to multiplex their outputs [12, 13]. For example, in a 40-nm digital CMOS process, two LC-VCOs (6–9 and 9–12 GHz) are needed to cover the required 6–12 GHz frequency range with sufficient phase-noise performance for SDR application in [14]. However, this method is not area efficient since the monolithic inductor occupies much larger chip area than other devices and is not scalable with CMOS technology.

To make the matter worse, the problem with insufficient tuning range of conventional LC-VCOs becomes more and more acute as the oscillation frequency keeps increasing. Since the varactor Q becomes dominantly low in the tank, the limited varactor size degrades the frequency tuning range greatly. The typical tuning range of LC-VCOs reported at around 60 GHz is less than 10 % [14–16], which is far from being sufficient to cover the 9-GHz bandwidth required by IEEE 802.11ad standard or IEEE 802.15.3c standard when taking into account process variations and inaccurate device modeling. Similarly, high-frequency LC-ILFDs suffer from a big